UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,342	12/03/2003	Anupam Anand	15098US01	9025

23446 7590 01/10/2007

MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER	
CAMPOS, YAIMA	
ART UNIT	PAPER NUMBER
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/726,342	ANAND, ANUPAM	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/726,342 has a total of 40 claims pending in the application; there are 5 independent claims and 35 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

III. OBJECTIONS TO THE SPECIFICATION

Claim Objections

4. Claims 10, 16 and 23 are objected to because of the following informalities:

The word "segment" in claim 10, line 2 appears to be a typographical error and should be corrected to read **-segments-**.

The words "bit map" in claims 16 and 23 appear to be a typographical error and should be changed to read **–bitmap-**.

Appropriate correction is required.

IV. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 1-3, 5-6, 8-16, 24-26, 30-35 and 37-39** are rejected under 35 U.S.C. 102(b) as being anticipated by Goldberg (US 6,874,062).

7. As per **claim 1**, Goldberg discloses

A memory management circuit for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management circuit comprising: **[Goldberg discloses "an Operating System (OS) 200 running on IP 104, manages and allocates the various resources of Data Processing System" (Col. 7, lines 11-13) wherein "Files can further be subdivided into smaller addressable portions of memory called "sections," wherein each section has a same predetermined size" (Col. 7, lines 22-26) and explains grouping sections into segments (Col. 8, lines 49-65) (Figures 1 and 2 and related text)]**

a first logic circuit associated with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when the first memory block has a memory segment that is available for data storage and a second state when the first memory block does not have a memory segment that is available for data storage **["in a hierarchical bitmap scheme... the**

Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) and explains "the LLB may be divided into Segments... these Segments all include a same predetermined number of bits... a bitmap is then created to define the Segments of the LLB. This bitmap, which may be referred to as Bitmap 1, will include a corresponding bit to describe an associated different one of the Segments of the LLB... indicating the availability of memory... a bit in Bitmap 1, is set to "0" if any of the bits in the corresponding LLB are also cleared. A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory... a bit in Bitmap 1 is set to "1" if all bits in the corresponding LLB Segment are set" (Col. 8, lines 49-65) (Figures 5-6 and related text) wherein "a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61)].

8. As per **claim 2**, Goldberg discloses the memory management circuit of claim 1, further comprising a second logic circuit associated with a first memory segment of the first memory block, the second logic circuit having a first state when the first memory segment is available for data storage and a second state when the first memory segment is not available for data storage **[Goldberg discloses "in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 trough 7... a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text)].**

9. As per **claim 3**, Goldberg discloses the memory management circuit of claim 1, wherein the first state and second state are states of a single logic bit **["a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61)]**.

10. As per **claims 5-6**, Goldberg discloses the memory management circuit of claim 1, further comprising a second logic circuit having a plurality of logic sub-circuits, each logic sub-circuit corresponding to a respective one of the memory segments of the first memory block, each logic sub-circuit having a first state when its respective memory segment is available for data storage and a second state when its respective memory segment is not available for data storage; further comprising a third logic circuit having a state indicative of a memory address of the first memory segment **["in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 trough 7... a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text). Goldberg further discloses "additional hierarchical levels within the bitmap may be created... bitmap 1 may be subdivided into Segments" (Col. 10, lines 34-37) (Figures 5-6 and related text)]**.

11. As per **claim 8**, Goldberg discloses the memory management circuit of claim 2, wherein the first and second states of the first logic circuit are states of a single logic bit and the first and second states of the second logic circuit are states of a single digital bit **["a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61)]**.

12. As per **claim 9**, Goldberg discloses the memory management circuit of claim 2, wherein the first state of the first logic circuit is indicative of a memory address of the first memory block and the first state of the second logic circuit is indicative of a memory offset between the memory address of the first memory block and the memory address of the first memory segment **[Goldberg discloses this limitation as in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 trough 7... a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text). Goldberg further discloses "additional hierarchical levels within the bitmap may be created... bitmap 1 may be subdivided into Segments" (Col. 10, lines 34-37) (Figures 5-6 and related text) and explains performing a top-down search of hierarchical bitmap structures in which "if such a string is located, processing continues... If an address is returned indicating that the desired available memory had been located, each of the bits in the Current_BML that corresponds to a bit described by Saved_Bits must be set to an appropriate state... the state indicated whether or not the bit corresponds to memory that has been entirely allocated" (Col. 14, lines 38-57) (Figures 8A-9D and related text)].**

13. As per **claim 10**, Goldberg discloses a memory management circuit for managing a memory having a first and second memory block, each memory block having a first and second memory segment, the memory management circuit comprising: **[Goldberg discloses "an Operating System (OS) 200 running on IP 104 manages and allocates the various resources**

of Data Processing System" (Col. 7, lines 11-13) wherein "Files can further be subdivided into smaller addressable portions of memory called "sections," wherein each section has a same predetermined size" (Col. 7, lines 22-26) and explains grouping sections into segments (Col. 8, lines 49-65) (Figures 1 and 2 and related text)]

a first logic circuit having a first state when any of the memory segments of the first memory block are available for data storage and a second state when none of the memory segments of the first memory block are available for storage; **["in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) and explains "the LLB may be divided into Segments... these Segments all include a same predetermined number of bits... a bitmap is then created to define the Segments of the LLB. This bitmap, which may be referred to as Bitmap 1, will include a corresponding bit to describe an associated different one of the Segments of the LLB... indicating the availability of memory... a bit in Bitmap 1, is set to "0" if any of the bits in the corresponding LLB are also cleared. A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory... a bit in Bitmap 1 is set to "1" if all bits in the corresponding LLB Segment are set" (Col. 8, lines 49-65) (Figures 5-6 and related text) wherein "a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61)]**

and a second logic circuit having a first state when any of the memory segments of the second memory block are available for data storage and a second state when none of the memory segments of the second memory block are available for data storage **[Goldberg discloses "in a**

hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 trough 7... a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text)].

14. As per **claims 11 and 12**, Goldberg discloses the memory management circuit of claim 10, further comprising: a third logic circuit having a first state when the first memory segment of the first memory block is available for data storage and a second state when the first memory segment of the first memory block is not available for data storage; and a fourth logic circuit having a first state when the second memory segment of the first memory block is available for data storage and a second state when the second memory segment of the first memory block is not available for data storage; further comprising: a fifth logic circuit having a first state when the first memory segment of the second memory block is available for data storage and a second state when the first memory segment of the second memory block is not available for data storage; and a sixth logic circuit having a first state when the second memory segment of the second memory block is available for data storage and a second state when the second memory segment of the second memory block is not available for data storage **["in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 trough 7... a bit is set if a Section is in use**

and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text). Goldberg further discloses "additional hierarchical levels within the bitmap may be created... bitmap 1 may be subdivided into Segments" (Col. 10, lines 34-37) (Figures 5-6 and related text)].

15. As per **claim 13**, Goldberg discloses a memory management system for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management system comprising: a first bitmap having a sequence of bits, each bit of the first bitmap corresponding to a respective one of the plurality of memory blocks, each bit of the first bitmap having a first logic state if the bit's respective memory block has a memory segment that is available for data storage and a second logic state if the bit's respective memory block does not have a memory segment that is available for data storage; and a second bitmap having a sequence of bits, each bit of the second bitmap corresponding to a respective one of the plurality of memory segments of the memory, each bit of the second bitmap having a first logic state if the bit's respective memory segment is available for data storage and a second logic state if the bit's respective memory segment is not available for data storage **[The same rationale in the rejection to claims 1 and 10 is herein incorporated]**.

16. As per **claim 14**, Goldberg discloses the memory management system of claim 13, further comprising a logic circuit that identifies a bit in the first bitmap having the first logic state **[Goldberg discloses this limitation as "an Operating System (OS) 200 running on IP 104 manages and allocates the various resources of Data Processing System" (Col. 7, lines 11-13) and explains performing a search for "an available storage Segment of a predetermined length" (Col. 11, lines 23-28) (Figures 8A-9D and related text)]**.

17. As per **claim 15**, Goldberg discloses the memory management system of claim 13, further comprising a logic circuit that identifies a memory block having a memory segment available for data storage by identifying a first bit in the first bitmap having a state indicative of the first bit's respective memory block having a memory segment available for data storage, and identifies a memory segment that is available for data storage by identifying a second bit in the second bitmap having a logic state indicative of the second bit's respective memory segment being available for data storage **[Goldberg discloses this limitation as "search mechanism for N contiguous available memory sections.... the search starts at one edge of the highest level in the HBS. The search looks for as many contiguous bits in the predetermined state as are required to satisfy the buffer requirements" (Col. 12, lines 28-48) (Figures 9A-9D and related text)]**.

18. As per **claim 16**, Goldberg discloses the memory management system of claim 15, wherein the logic circuit identifies the second bit in the second bitmap by analyzing only bits in the second bit map that correspond to memory segments in the identified memory block **[Goldberg discloses this limitation as "if the current BML is the LLB, processing proceeds... a determination is made as to whether a contiguous group of N bits is set to the predetermined sate indicating available memory. If so, the bits are set to the state indicating the memory is now unavailable... if no set of bits may be located indicating the availability of the desired memory, a return to the calling set of instructions is executed" (Col. 14, line 66-Col. 15, line 11) (Figures 9A-9D and related text)]**.

19. As per **claim 24**, Goldberg discloses a method for managing memory, the method comprising: analyzing a first flag to determine whether a block of memory segments includes a

memory segment that is available for data storage; and if the block of memory segments includes a memory segment that is available for data storage, identifying a memory segment in the block of memory segments that is available for data storage **[Goldberg discloses this limitation as "an Operating System (OS) 200 running on IP 104 manages and allocates the various resources of Data Processing System" (Col. 7, lines 11-13) wherein "in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) and explains "the LLB may be divided into Segments... these Segments all include a same predetermined number of bits... a bitmap is then created to define the Segments of the LLB. This bitmap, which may be referred to as Bitmap 1, will include a corresponding bit to describe an associated different one of the Segments of the LLB... indicating the availability of memory... a bit in Bitmap 1, is set to "0" if any of the bits in the corresponding LLB are also cleared. A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory... a bit in Bitmap 1 is set to "1" if all bits in the corresponding LLB Segment are set" (Col. 8, lines 49-65) (Figures 5-6 and related text) wherein "a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) and explains performing "a search for an available storage Segment of a predetermined length" (Col. 11, lines 23-28) (Figures 8A-9D and related text)].**

20. As per **claim 25**, Goldberg discloses the method of claim 24, wherein identifying a memory segment in the block of memory segments that is available for data storage comprises analyzing a second flag to determine whether a particular memory segment in the block of

memory segments is available for data storage **[With respect to this limitation, Goldberg disclsoes "the HBS may be used to locate an available storage Segment of a predetermined length" (Col. 11, lines 23-28) (Figures 8A-9D and related text)]**.

21. As per **claim 26**, Goldberg disclsoes the method of claim 24, wherein identifying a memory segment in the block of memory segments that is available for data storage comprises: analyzing a second flag to determine whether a first memory segment in the block of memory segments is available for data storage; if the first memory segment in the block of memory segments is available for data storage, determining the address of the first memory segment; and if the first memory segment in the block of memory segments is not available for data storage, analyzing a third flag to determine whether a second memory segment in the block of memory segments is available for data storage **[With respect to this limitation, Goldberg discloses "the HBS may be used to locate an available storage Segment of a predetermined length" (Col. 11, lines 23-28) (Figures 8A-9D and related text) "in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 trough 7... a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text). Goldberg further discloses "additional hierarchical levels within the bitmap may be created... bitmap 1 may be subdivided into Segments" (Col. 10, lines 34-37) (Figures 5-6 and related text)]**.

22. As per **claim 30**, Goldberg discloses the method of claim 24, wherein identifying a memory segment in the block of memory segments that is available for data storage comprises analyzing a set of flags, each flag corresponding to a respective memory segment in the block of memory segments, to identify a memory segment in the block of memory segments that is available for data storage **[The rationale in the rejection to claim 24 is herein incorported]**.

23. As per **claim 31**, Goldberg discloses the method of claim 24, further comprising: if the block of memory segments does not include a memory segment that is available for data storage, analyzing a second flag to determine whether a second block of memory segments includes a memory segment that is available for data storage; and if the second block of memory segments includes a memory segment that is available for data storage, identifying a memory segment in the second block of memory segments that is available for data storage **[With respect to this limitation, Goldberg discloses "the HBS may be used to locate an available storage Segment of a predetermined length" (Col. 11, lines 23-28) (Figures 8A-9D and related text) "in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 trough 7... a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text). Goldberg further discloses "additional hierarchical levels within the bitmap may be created... bitmap 1 may be subdivided into Segments" (Col. 10, lines 34-37) (Figures 5-6 and related text)]**.

24. As per **claim 32**, Goldberd discloses the method for managing a memory, the memory having a plurality of memory blocks, each of the plurality of memory blocks having a plurality of memory segments, the method comprising: representing each of the plurality of memory blocks with a respective bit in a first bitmap, the logic state of each respective bit in the first bitmap indicative of whether each bit's respective memory block has at least one memory segment that is available for data storage; and representing each of the memory segments with a respective bit in a second bitmap, the logic state of each respective bit in the second bitmap indicative of whether each bit's respective memory segment is available for data storage **[The same rationale in the rejection to claims 1, 10 and 13 is herein incorporated]**.

25. As per **claims 33 and 34**, Goldberg discloses the method of claim 32, further comprising identifying a memory block that has a memory segment available for data storage by locating a bit in the first bitmap that has a logic state indicative of the memory block having a memory segment available for data storage; further comprising identifying a memory segment that is available for data storage by locating a bit in the second bitmap that has a logic state indicative of the memory segment being available for data storage **["the HBS may be used to locate an available storage Segment of a predetermined length" (Col. 11, lines 23-28) (Figures 8A-9D and related text) "in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 trough 7... a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text). Goldberg further discloses "additional hierarchical**

levels within the bitmap may be created... bitmap 1 may be subdivided into Segments" (Col. 10, lines 34-37) (Figures 5-6 and related text)].

26. As per **claim 35**, Goldberg discloses the method of claim 34, wherein locating a bit in the second bitmap that has a logic state indicative of the memory segment being available for data storage comprises: identifying the position of the bit in the first bitmap that corresponds to the identified memory block; utilizing the position of the bit in the first bitmap to index to a location in the second bitmap at which the bits corresponding to the memory segments in the identified memory block are located; and analyzing at least one of the bits corresponding to the memory segments in the identified memory block to identify a bit that has a logic state indicative of the bit's respective memory segment being available for data storage **[Goldberg discloses this limitation as searching hierarchical bitmap structures for an available memory buffer/segment of a predetermined size (Figures 8A-9D and related text)]**.

27. As per **claim 37**, Goldberg discloses the method of claim 32, further comprising designating that a memory segment is available for data storage by determining a position of a bit in the first bitmap that corresponds to a memory block that includes the memory segment, and setting the bit in the first bitmap to a logic state indicative of the memory block having a memory segment available for data storage**["in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) and explains "the LLB may be divided into Segments... these Segments all include a same predetermined number of bits... a bitmap is then created to define the Segments of the LLB. This bitmap, which may be referred to as Bitmap 1, will include a corresponding**

bit to describe an associated different one of the Segments of the LLB... indicating the availability of memory... a bit in Bitmap 1, is set to "0" if any of the bits in the corresponding LLB are also cleared. A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory... a bit in Bitmap 1 is set to "1" if all bits in the corresponding LLB Segment are set" (Col. 8, lines 49-65) (Figures 5-6 and related text) wherein "a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61)].

28. As per **claims 38-39**, Goldberg discloses the method of claim 32, further comprising designating that a memory segment is available for data storage by determining a position of a bit in the second bitmap that corresponds to the memory segment, and setting the bit in the second bitmap to a logic state indicative of the memory segment being available for data storage; further comprising designating that a memory segment is available for data storage by determining a position of a bit in the second bitmap that corresponds to the memory segment, and setting the bit in the second bitmap to a logic state indicative of the memory segment being available for data storage **[Goldberg discloses this limitation as "A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory... a bit in Bitmap 1 is set to "1" if all bits in the corresponding LLB Segment are set" (Col. 8, lines 49-65) (Figures 5-6 and related text)]**.

Claim Rejections - 35 USC § 103

29. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

30. **Claims 4 and 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Goldberg (US 6,874,062) in view of Lehman (US 6,658,437).

31. As per **claim 4**, Goldberg discloses the memory management circuit of claim 1, but does not explicitly disclose the details of having the first state includes at least a portion of a memory address of the first memory block.

Lehman discloses having the first state includes at least a portion of a memory address of the first memory block as **["blocks larger than 1 can start only on an appropriate block address... the bit string 1111 1100 0000 0011, represents one allocated block of size 4, one allocated block of size 2, one free block of size 2, one free block of size 4, one free block of size 2, and one allocated block of size two" (Col. 11, lines 38-46) (Figure 7 and related text) and explains "the address of a block is determined by the bit position in the base group and by the position of the base group in the larger allocation array" (Col. 10, line 61-Col. 11, line 5) (Figure 9 and related text)]**.

Goldberg (US 6,874,062) and Lehman (US 6,658,437) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory management circuit of claim 1 as taught by Goldberg and further the first state includes at least a portion of a memory address of the first memory block as taught by Lehman.

The motivation for doing so would have been because Lehman discloses **["a data space management system that requires less space to store allocation information in order to**

increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions" (Col. 2, lines 42-48)].

Therefore, it would have been obvious to combine Lehman (US 6,658,437) with Goldberg (US 6,874,062) for the benefit of creating a memory management cicuit to obtain the invention as specified in claim 4.

32. As per **claim 7**, Goldberg discloses the memory management circuit of claim 2, and explains **[Goldberg discloses this limitation as in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 trough 7... a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text). Goldberg further discloses "additional hierarchical levels within the bitmap may be created... bitmap 1 may be subdivided into Segments" (Col. 10, lines 34-37) (Figures 5-6 and related text) and explains performing a top-down search of hierarchical bitmap structures in which "if such a string is located, processing continues... If an address is returned indicating that the desired available memory had been located, each of the bits in the Current_BML that corresponds to a bit described by Saved_Bits must be set to an appropriate state... the state indicated whether or not the bit corresponds to memory that has been entirely allocated" (Col. 14, lines 38-57) (Figures 8A-9D and related text)]** but does not explicitly disclose the details of a third logic circuit that converts the first state of the first

logic circuit and the first state of the second logic circuit to the memory address of the first memory segment.

Lehman discloses a third logic circuit that converts the first state of the first logic circuit and the first state of the second logic circuit to the memory address of the first memory segment as **["blocks larger than 1 can start only on an appropriate block address... the bit string 1111 1100 0000 0011, represents one allocated block of size 4, one allocated block of size 2, one free block of size 2, one free block of size 4, one free block of size 2, and one allocated block of size two" (Col. 11, lines 38-46) (Figure 7 and related text) and explains "the address of a block is determined by the bit position in the base group and by the position of the base group in the larger allocation array" (Col. 10, line 61-Col. 11, line 5) (Figure 9 and related text)]**.

Goldberg (US 6,874,062) and Lehman (US 6,658,437) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory management circuit of claim 1 as taught by Goldberg and further have a third logic circuit that converts the first state of the first logic circuit and the first state of the second logic circuit to the memory address of the first memory segment..

The motivation for doing so would have been because Lehman discloses **["a data space management system that requires less space to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions" (Col. 2, lines 42-48)]**.

Therefore, it would have been obvious to combine Lehman (US 6,658,437) with Goldberg (US 6,874,062) for the benefit of creating a memory management cicuit to obtain the invention as specified in claim 7.

33. **Claims 17-23, 27-29, 36 and 40** is rejected under 35 U.S.C. 103(a) as being unpatentable over Goldberg (US 6,874,062) in view of Lehman (US 6,658,437) and Dhong et al. (6,430,672).

34. As per **claims 17-23, 27-29, 36 and 40**, Goldberg discloses the memory management system of claim 15, but does not explicitly disclose wherein the logic circuit determines the address of the memory segment that is available for data storage by generating a most significant portion of the address according to the position of the first bit in the first bitmap sequence of bits, and generating a least significant portion of the address according to the position of the second bit in the second bitmap sequence of bits.

Lehman discloses a generating portions of the address according to availability information stored in a bitmap as **["blocks larger than 1 can start only on an appropriate block address... the bit string 1111 1100 0000 0011, represents one allocated block of size 4, one allocated block of size 2, one free block of size 2, one free block of size 4, one free block of size 2, and one allocated block of size two" (Col. 11, lines 38-46) (Figure 7 and related text) and explains "the address of a block is determined by the bit position in the base group and by the position of the base group in the larger allocation array" (Col. 10, line 61-Col. 11, line 5) (Figure 9 and related text)]** but does not disclose expressly the details of having a block portion of an address as a most significant portion and a segment portion of an address as a least significant portion.

Dhong discloses having a block portion of an address as a most significant portion and a segment portion of an address as a least significant portion as **[address mapping for a system memory in which "a line is the part of a memory bank that consists of a number of storage locations that can be addressed as a whole by a line-number or bank-internal address... the most significant address bits of a physical address constitute a block address, and they are identical for the same block... block offset 14 represents a certain point within a block... the least significant bits of a page offset 12 are used as block offset 14, and the remaining bits of page offset 12 are used as the least significant bits for block address 13" (Col. 1, lines 27-56) wherein "the output of lookup table 33 is utilized to form the least significant bits of a bank number and the output of lookup table 34 is utilized to form the most significant bits of the bank number" (Col. 4, lines 7-21)]**.

Goldberg (US 6,874,062), Lehman (US 6,658,437) and Dhong et al. (6,430,672) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory management circuit of claim 1 as taught by Goldberg and further generating portions of the address according to availability information stored in a bitmap as taught by Lehman and further having a block portion of an address as a most significant portion and a segment portion of an address as a least significant portion as taught by Dhong.

The motivation for doing so would have been because Lehman discloses **["a data space management system that requires less space to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data**

values, and also to free up space for use in other control functions" (Col. 2, lines 42-48)] and Dohng discloses **["an improved method for performing address mapping to access information stored in a memory" (Col. 2, lines 31-33)]**.

Therefore, it would have been obvious to combine Dhong et al. (6,430,672) with Goldberg (US 6,874,062) and Lehman (US 6,658,437) for the benefit of creating a memory management cicuit to obtain the invention as specified in claims 17-23, 27-29, 36 and 40.

VI RELEVANT ART CITED BY THE EXAMINER

35. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

36. The following references teaches dynamic disk space management by multiple database server instances in a cluster configuration.

U.S. PATENT NUMBER

US 2003/0220951

VII. CLOSING COMMENTS

Examiner's Note

Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from

the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

37. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

38. Per the instant office action, claims 1-40 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

40. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained

from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 6, 2007

Yaima Campos
Examiner
Art Unit 2185

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100